when $L_{BE}$ = 0.2μm, the electron accumulation in the base region is suppressed, compared to when $L_{BE}$ = 1μm. This is attributed to the fact that electrons which should accumulate in the external base region are absorbed in the base electrode with shorter $L_{BE}$. Therefore, $\tau_B$, given by $(\partial Q_{nB}/\partial I_C)_{V_{CE}}$, becomes shorter, resulting in the higher $f_T$.

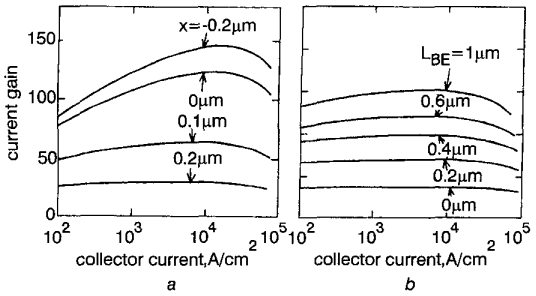


**Fig. 4** *Calculated current gain $h_{FE}$ against $I_C$*

*a* Different values of $x$
$V_{CE}$ = 1.5V, $L_{BE}$ = 1μm
*b* Different values of $L_{BE}$
$V_{CE}$ = 1.5V, $x$ = 0.2μm

Here, there is one point to be noted. When the accumulating electrons are absorbed in the base electrode, the base current $I_B$ increases. Fig. 4 shows the calculated current gain $h_{FE}$ ($I_C/I_B$) against $I_C$ for different values of $x$ and $L_{BE}$. From Fig. 4*b*, we see that as $L_{BE}$ becomes shorter, $h_{FE}$ becomes lower because of the increase in $I_B$. High $h_{FE}$ is achieved by setting $x$ negative (and avoiding carrier blocking), as shown in Fig. 4*a*. Therefore, we can say that to maintain high $f_T$ and $h_{FE}$ in collector-up HBTs, the collector width should be made wider than the intrinsic emitter width.

In summary, we have studied the effects of carrier-blocking on the cutoff frequency characteristics of collector-up AlGaAs/GaAs HBTs. It is shown that, by putting the base electrode closer to the intrinsic collector, the carrier-blocking effect is reduced and $f_T$ is maintained rather high, although the current gain $h_{FE}$ may degrade because of the increase in base current. To keep both $f_T$ and $h_{FE}$ high, the collector width should be made wider than the emitter width.


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## References

1 ASBECK, P.M., CHANG, M.F., WANG, K.C., SULLIVAN, G.J., and CHEUNG, D.T.: 'GaAs-based heterojunction bipolar transistor for very high performance electronic circuits', *Proc. IEEE*, 1993, **81**, pp. 1706–1726

2 ISHIBASHI, T., and YAMAUCHI, Y.: 'A possible near-ballistic collection in an AlGaAs/GaAs HBT with a modified collector structure', *IEEE Trans. Electron. Devices*, 1988, **ED-35**, pp. 401–404

3 HORIO, K., IWATSU, Y., and YANAI, H.: 'Numerical simulation of AlGaAs/GaAs heterojunction bipolar transistors (HBTs) with various collector parameters', *IEEE Trans. Electron Devices*, 1989, **ED-36**, pp. 617–624

4 YAMAHATA, S., MATSUOKA, Y., and ISHIBASHI, T.: 'High-$f_{max}$ collector-up AlGaAs/GaAs heterojunction bipolar transistors with a heavily carbon-doped base fabricated using oxygen-ion implantation', *IEEE Electron Device Lett.*, 1993, **14**, pp. 173–175

5 HORIO, K., and NAKATANI, A.: 'Analysis of carrier-blocking effect in AlGaAs/GaAs HBTs with insulating external collector and design criteria for collector-up HBTs', *IEEE Trans. Electron Devices*, 1995, **ED-42**, pp. 1897–1902

# Multiplexing architecture for mixed-signal CMOS fuzzy controllers

F. Vidal-Verdú, R. Navas-González and A. Rodríguez-Vázquez

Limited precision imposes limits on the complexity of analogue circuits, and hence fuzzy analogue controllers are usually oriented to fast low-power systems with low-medium complexity. A strategy to preserve most of the advantages of an analogue implementation, while allowing a marked increment in system complexity, is presented.

*Introduction:* Because analogue fuzzy controllers operate in fully parallel mode, they are well suited for applications that require high operation speed. However, the most complex monolithic analogue controller chips reported to date feature 13-rule at 3-input [1] and 16-rule at 2-input [2], which is much smaller than the up to 100-rule and 4-input reported for digital chips [3].

A major obstacle to increasing the complexity of fully-analogue controller chips is the existence of global computation nodes where the errors caused by the rule antecedent circuits are aggregated; for instance, the centre of gravity is evaluated in such a node. This obstacle is particularly pertinent for those architectures based on lattice partitions of the universe of discourse because these partitions (which are otherwise advantageous for control applications [4]) make the rule count increase exponentially with the input count. Thus, the accumulated error also increases exponentially, and the system architecture may become unfeasible even for low numbers of inputs.

This Letter presents a novel mixed-signal controller chip architecture which maintains the fully-parallel operation feature of analogue chips but obtains the accumulated error independently of the number of rules. It takes advantage of the fact that each fuzzy rule influences the system output only inside a local, limited region of the universe of discourse. Consequently, the universe of discourse can be split into sub-regions and the output for each sub-region can be calculated by only evaluating a reduced number of fuzzy rules (called active rules [5]). This number is the same for each sub-region, but the corresponding rule parameters differ from one region to another. Our proposal implements this reduced number of rules by a low-dimension programmable analogue processor, and employs multiplexing to cover the entire universe of discourse. On chip digital circuits are employed for multiplexing and for programmability.

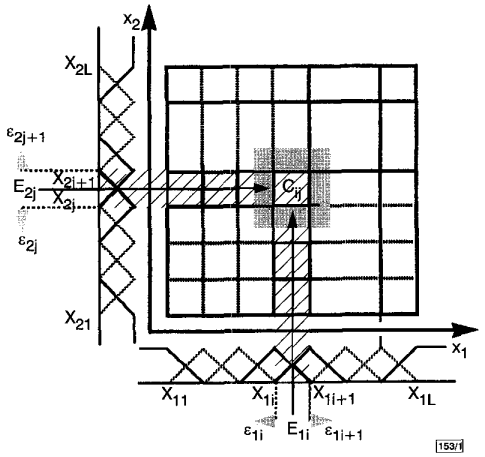


**Fig. 1** *Universe of discourse split into interpolation intervals*

*Architecture and functional description:* Consider the bi-dimensional lattice partition in Fig. 1. It shows the universe of discourse split into interpolation intervals, each having a different set of active rules. For instance, any input pair $(x_1, x_2)$ in the hatched interval $C_{ij} = [(\varepsilon_{1i}, \varepsilon_{1i+1}) \times (\varepsilon_{2i}, \varepsilon_{2i+1})]$ maps onto an output determined by the rules in the shaded interval (active rules) while all remaining rules have no influence on the output. Only the active rule membership functions and their associated singleton values are needed for the interpolation procedure. In addition, the only

membership function pieces needed are those which actually contribute to the system output. Thus, in the case illustrated in Fig. 1, only the pieces drawn with heavy lines and the singletons associated with the four active rule consequents, $y^*_{ij}$, $y^*_{i(j+1)}$, $y^*_{(i+1)j}$ and $y^*_{(i+1)(j+1)}$ are needed to generate the output in the interval $C_{ij}$.

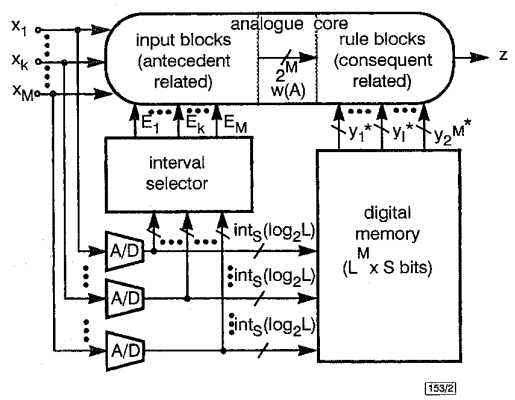


**Fig. 2** *Proposed architecture*

Fig. 2 shows the proposed architecture for a controller with $M$ inputs, $L$ labels per input (thus $L^M$ rules), and $S$ bits per singleton. It comprises the following blocks:

(i) *A/D converters*: Their function is to encode the interpolation interval $C_{ij}$ associated with the current input. There are $M$ A/D converters, one per input, with a resolution equal to the next superior integer $\log_2 L$, i.e. $int_s(\log_2 L)$. Thus, this battery of converters provides a word of $M[int_s(\log_2 L)]$ bits that drives the interval selector block and the digital memory block.

(ii) *Interval selector*: This selects a set of voltage values $E_1$, ..., $E_k$, ..., $E_M$ to drive the analogue core and, thus, makes it implement the active membership functions.

(iii) *Digital memory:* This selects the active singleton programming values $y_1^*$, ..., $y_l^*$, ..., $y_{2^M}^*$ that configure the rule block of the analogue core consequents of the active rules. These are digital words of as many bits as needed to encode the required set of singleton values.

(iv) *Analogue core*: This performs the fuzzy computation, having a set of programming inputs which are driven by the interval selector and the digital memory blocks. These inputs set up the analogue core to work with the rule set that determines the system output, which means specifying the membership functions associated with the rule antecedents as well as the singleton values related to the consequents. The internal architecture of the analogue core is the same as for the fuzzy controller in [2], but only $2^M$ rules are needed here, and only two membership functions per input.

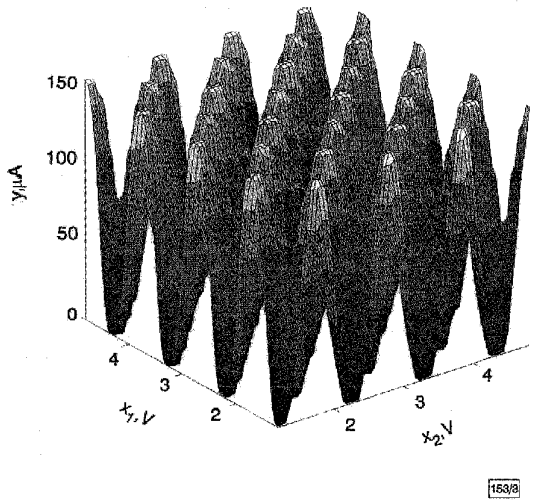


**Fig. 3** *DC surface response of example controller*

*Results and conclusions:* An example 64-rule, 2-input, 4 bit singleton controller ($L$ = 8, $M$ = 2 and $S$ = 4) has been designed in a CMOS 0.7 μm technology to demonstrate the viability of the proposed architecture.

High-speed flash A/D converters are used for interval encoding. The poly-silicon resistor array used to generate the converter thresholds is also exploited to generate the interval selector voltages. Thus, this latter block includes only analogue switches and some logic. The memory block is designed carefully so that the data are put in the singleton programming bus in the proper order - this is necessary to reduce the memory size by a factor of four. Finally, the 4-rule 2-input processing core is constructed by using building blocks similar to those presented in [2].

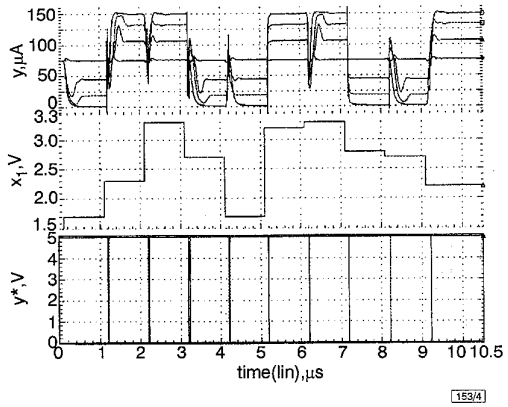


**Fig. 4** *Controller transient behaviour*

Fig. 3 shows the DC surface response of the controller for a case where the singletons are chosen to clearly display all the interpolation points. The DC accuracy was ~1%. Fig. 4 illustrates the controller transient behaviour for different values of $x_2$ (2.8, 2.9, 2.95 and 3 V), forcing $x_1$ to change for each of these values. The input was chosen so that the trajectory goes through different subregions. The delay time, including the time required for dynamic reconfiguration, is ~500 ns. The chip power consumption is 16 mW.

It is illustrative to compare the speed, area and power of this mixed-signal controller to that of a pure analogue controller with the same number of inputs and rules and digitally-programmable singletons. Assuming that the singletons are encoded with the same number of bits, the size of the digital memory is the same for the two controllers. However, while the number of rule blocks is $L^M$ for the fully-analogue controller, it is only $2^M$ for the new controller. The larger the ratio $\alpha = (L/2)^M$, the more advantageous and less error-prone is the new architecture as compared to a fully-analogue controller. Thus, while the circuit in [2] (designed in a 1 μm technology) comprises 16 rules with 470 ns delay, 8.6 mW power consumption and 1.6 mm² area, the example controller implements 64 rules with almost the same delay, 16 mW power and only 1 mm² area.

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## References

1 GUO, S., PETERS, L., and SURMANN, H.: 'Design and application of an analog fuzzy logic controller', *IEEE Trans. Fuzzy Syst.*, 1996, **4**, pp. 429–438

2 VIDAL-VERDÚ, F., NAVAS, R., and RODRÍGUEZ-VÁZQUEZ, A.: 'A 16 rules @2.5 Mflips mixed-signal programmable fuzzy controller CMOS-1 μm chip'. Proc. ESSCIRC'96, 1996, pp. 156–159

3 COSTA, A., DE GLORIA, A., FARABOSCHI, P., PAGNI, A., and RIZZOTTO, G.: 'Hardware solutions for fuzzy control', *Proc. IEEE*, 1995, **83**, pp. 422–434

4 BROWN, M., and HARRIS, C.: 'Neuro-fuzzy adaptive modeling and control' (Prentice Hall, Englewood Cliffs, 1994)

5 MASETTI, M., GANDOLFI, E., GABRIELI, A., and BOSCHETTI, F.: '4 input VLSI fuzzy chip design able to process an input data set every 320ns'. Proc. JCIS'95, Wrightsville Beach, North Carolina, USA, October 1995

## Errata

GREENSTEIN, L.J., ERCEG, V., and MICHELSON, D.G.: 'Modelling diversity reception over narrowband fixed wireless channels', *Electron. Lett.*, 1998, **34**, (11), pp. 1146–1147

*Editor's correction*

The names of the authors of this Letter were given in the wrong order. The correct list of authors is:

GREENSTEIN, L.J., MICHELSON, D.G., and ERCEG, V.

WE-SHYANG CHEN, CHUN-KUN WU, and KIN-LU WONG: 'Single-feed square-ring microstrip antenna with truncated corners for compact circular polarisation operation', *Electron. Lett.*, 1998, **34**, (11), pp. 1045–1047

*Editor's correction*

The name of the first author of this Letter was spelt incorrectly. The correct spelling is:

WEN-SHYANG CHEN

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